DESIGNAND ANALYSIS OF CLASS-EPOWER AMPLIFIER: A 4GHz BANDFOR MOBILE APPLICATION

BY

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DECLARATION

I hereby declare that this work is the product of my research efforts undertaken under the supervision of Dr. Auwalu Musa and has not been presented anywhere for the award of Master of Science (M.Sc) in Electronics. All the sources have been duly acknowledged.

……..

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CERTIFICATION

This is to certify that the research work for this dissertation and subsequent write-up by "Nasiru Abubakar (SPS/15/MPY/00054)" were carried out under my supervision.

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APPROVAL PAGE

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DEDICATION

I dedicate this dissertation to my mother Khadija Abubakar, my wife Maryam Nasiru, and my father Prof. B.G. Danshehu with my brother Abubakar Abubakar Gwadangaji.

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LIST OF ACRONYMS

ADS: Advanced Design System

AMPS: Advance Mobile Phone System

VHF: Very High Frequency

WLAN: Wireless local area network

IC: Integrated Circuit

RF: Radio Frequency

PA: Power Amplifier

CMOS: Complementary metal–oxide–semiconductor

GaAs: Gallium Arsenide

SiGe: Silicon-Germanium

SC: Short Channel

PAE: Power-Added-Efficiency

NMOSFET: n-channel metal–oxide–semiconductor Field Effect Transistor

SOC: System on Chip

ZVS:Zero Voltage Switching

ZVDS:Zero Voltage Derivative Switching

RF: Radio Frequency

ABSTRACT

The power amplifier(PA) is the most important component used for overall Radio frequency (RF) transmitter efficiency, because it consumes the largest portion of DC power in the transmitter. Highly efficient PAs are necessaryto improve overall efficiency.A class-E power amplifier is nonlinear amplifier, in the sense that variations ininput signal amplitude will not be reproduce at the output in any acceptable form.In this research efficient class-E power amplifier without excessive reactance at frequency was designed by using 180nm technology.The value of the efficiency obtained for the designed amplifier are 100%, for calculation98.42% for simulation and 90.34% for experimental powered with 1.8V DC. The amplifier was operated at band frequency of 4GHz and 50% duty cycle for a stablesinusoidal signal. The band frequency and duty cycle was so selected to optimize efficiency. At end of the research a design of 37.4mW Class-E power amplifier was achieved, and tested in the laboratory. An IRF540 NMOSFET was used in the design of the amplifier. Performance parameters relationships with Class-E power amplifier were observed and analysed in respect to the load and duty cycle. In wireless communication devices application, our design Class-E power amplifier shows a better performance and high efficiency at low power consumption by reducing the input DC power level (0.038W).Theoretical calculations, simulation and experimental results for optimum operation using selected component values were compared with other work, for industrial applications. Therefore the comparison is only base on 180nm technology which shows a better performance and high efficiency on our design.

CHAPTER ONE

INTRODUCTION

1.1 GENERAL INTRODUCTION

A power amplifier is an amplifier, which is capableof providing a large amount of power to the load such as loudspeaker, or motor. It is essential in almost all electronic systems where a large amount of power is supplied to the load. The PA is more commonly known as audio amplifier (Shankar *et al.,* 2016). It will be interesting to know that a power amplifier does not actually amplify the power. Rather it takes power from the DC power supply connected to the output circuit and convert it into useful AC signal power (Yusop *et al.,* 2016). The power is fed to the load.

Mobile equipment demands highly efficient Redio frequency (RF) transmitters to conserve battery life. Thus, highly efficient PAs are necessaryto improve overall efficiency. A class-E PA is suitable for a high-efficiency transmitter due to its high performance and simplicity. This type of amplifier with a shunt capacitor was first introduced by Sokal in 1975 and was examined by Raab 1977 in an analysis of idealized operation. The expensive development of wireless communication systems during the last decade has particularly put the design of RF PA in focus. Efficiency and linearity are opposing requirementsin the power amplifiers design and much research is focused on how to improve the efficiency of power amplifiers circuits while still satisfying the linearity requirements of a given system (Su *et al*., 1998 and Lee *et al*., 2004).

The need for linear power amplifiers arises in many radio frequency applications. At present, most linear PAs designed for portable devices, employ a class A output stage

andexhibit efficiencies around 30% to 40%(Razafi *et al.,* 1998). In this range of frequency in portable device Class- E amplifier has shown to exhibit efficiency as high as 96% (Sokal, 1975). To achieve a higher efficiency, it is possible to begin with a nonlinear power amplifier and apply linearization techniques to the circuit. The type of AC power developed at the output of a DC power amplifier is controlled by the input signal. Thus it is said that power amplifier is a DC to AC power converter whose action is controlled by the input signal. The power amplifiers are also known as large signal amplifiers (Saad *et al*., 2009).

To reduce power consumption and improve efficiency (Supriya and Ananda, 2015). Class-E amplifiers have been shown to be usable at higher frequencies and useful for wireless communications. And also they have been shown to have much better performance and efficiency than other classes of power amplifiers at lower supply voltages (Sowlati, 1996)

1.2 MOTIVATION

- To design and obtain an amplifier the will provide high efficiency at high frequency. Also to be less sensitive to the transition time of the switch.
- To get amplifiers that can be designed with a small size, light weight and relatively tolerance to circuit variation.
- It was shown that Class E amplifier is the most efficient inverter so far, because of its ability to achieve zero voltage switching.
- This informs the selection of Class E amplifier over other Classes of operation. As the project aims in achieving the high efficiency of PA the option of ClassE is the better choice for the work to becarried out.

1.3 STATEMENT OF THE PROBLEM

Most of high loss of power is usually verified in the active device that function as a switch, and other problems are: Power dissipation in the active device, Variation in supply voltage and Inductance constraint using Narrow band Class-E power amplifier design. To obtain high efficiency the current and voltage waveform are displaced with respect to time.

1.4 AIM AND OBJECTIVES

1.4.1 AIM

The main aim of this research is to design and verify different performance parameters of Class E power amplifier.

1.4.2 OBJECTIVES

The objectives of the research work are as follows:

- **i.** To design and simulate an efficient power amplifier to be used in range of4GHz Bandfor wireless Communication.
- **ii.** To calculate the performance parameters relationship of Class-E power amplifier. Some of the parameters to be investigated are; maximum power output, efficiency e.t.c.
- **iii.** To compare the calculated values with experimental and available results.
- **iv.** To improve the efficiency in the design specifically at4GHz band.

1.5 SCOPE AND LIMITATION

1.5.1 SCOPE

The work is restricted to a 4GHz band only using a Class-E PA. Other Classes of PA were only analysed for comparative study.

1.5.2 LIMITATION

The research is limited to a Narrowband amplifier designof ClassE power amplifier with the objective of achieving high efficiency at low power consumption by reducing the input DC power level using 180nm technology.

CHAPTER TWO

LITERATURE REVIEW

2.1 HISTORICAL BACKGROUND

A Class-E amplifier for RF communication was first presented to the scientific community by Sokal in 1975. Prior to that, the applications of class-E amplifiers were limited to the very high frequency (VHF) band. At this range of frequency, class- E amplifier has shown to exhibit efficiencies as high as 96% (Sokal, 1975). Few years later, it was observed that Class E amplifiers can also be used at higher frequencies (Sowlati *et al.,* 1996). Several papers have reported class- E amplifiers operation at a frequency above the VHF band (Mader *et al.,* 1998). As mentioned earlier, a class-E is nonlinear amplifier, in the sense that variations ininput signal amplitude will not be reproduced at the output in any acceptable form. Moreover, class-E amplifier configurations prove to have higher efficiency with simpler circuits than conventional reduced conduction angle classes. The assumptions of the circuit are quite similar to the one that is presented in (Sokal, 1975).

2.2 LITERATURE REVIEW

The switching behaviour of Class-E PA was observed in the work of Zhisheng *et al.,* (2012). The losses in Class-E amplifier with DC feed inductancewere analysed. By the combination of a dynamic supply voltage and a dynamic cascode bias voltage,high drain efficiency is achieved over a wide powercontrol range, covering from 2.2 up to 20dBm. Fast envelope switching is obtained by adding a single switch to the common-gate nodes of both the Class-E stage and the second driver stage. The design of theart of work was done at 2.45GHz differential cascode ClassE PA in

0.18μm CMOS with onchip DC-feed inductor. At 20dBm, a power-added efficiency as high as 43.6% was measured.

However, Frederickh and Raab, (1977) presented another idea of theclass E tune power amplifier which consists of a load network and a single transistor that is operated as aswitch at the carrier frequency of the output signal. The simplest type ofload network consists of a capacitor shunting the transistor and a series tuned output circuit with residual reactance. Circuit operation is determined by the transistor when it is on, and by the transient response of the load network when the transistor is off. The basic equations governing amplifier operation are derived using Fourier series techniques and a high-Qassumption.

Also, Sokal, (1975) introduced the idea of new class of high efficiency tuned single ended switching Power Amplifiers. The amplifiers is described based on a load network synthesize to the transient response. The circuit maximizes power efficiency even if the active device switching times are substantial fractions of the AC cycle. The Class E amplifier type is illustrated in Figure 2.2

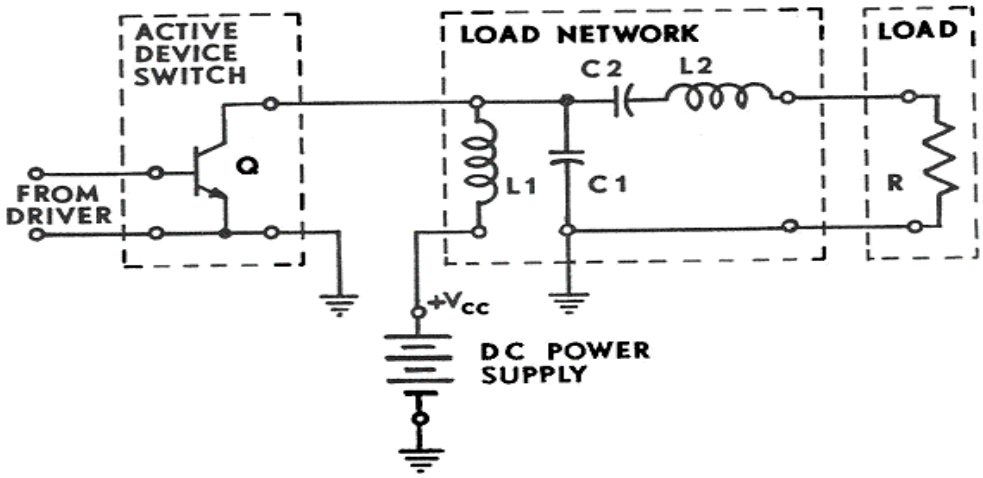


Figure 2.2 Schematic of low-order Class-E amplifier

Kenle *et al.,* (2011) presented clear idea of the Broadband Class-E amplifier designs. They proposed a new design methodology for the designing and implementing of efficiency broadband ClassE PA using high order low pass filter prototype. GaN transistor has beencharacterized and modelled to perform the operation under broad band Class-E amplifier. The circuit is accompanied with matching network (see Figure 2.2). A sixth order low pass filter matching network was designed and implemented to suit output matching,which provides optimized fundamental and harmonic impedances within an octave bandwidth. Power amplifier isrealized from 1.2 to 2GHz with an efficiency between 80%-89%, which is said to be the highest reported today for such a bandwidth. An overall PA bandwidth of 0.9- 2.2GHz is measured with 10-20W output power, 10-13dB gain and 63%-89% efficiency through out the band.

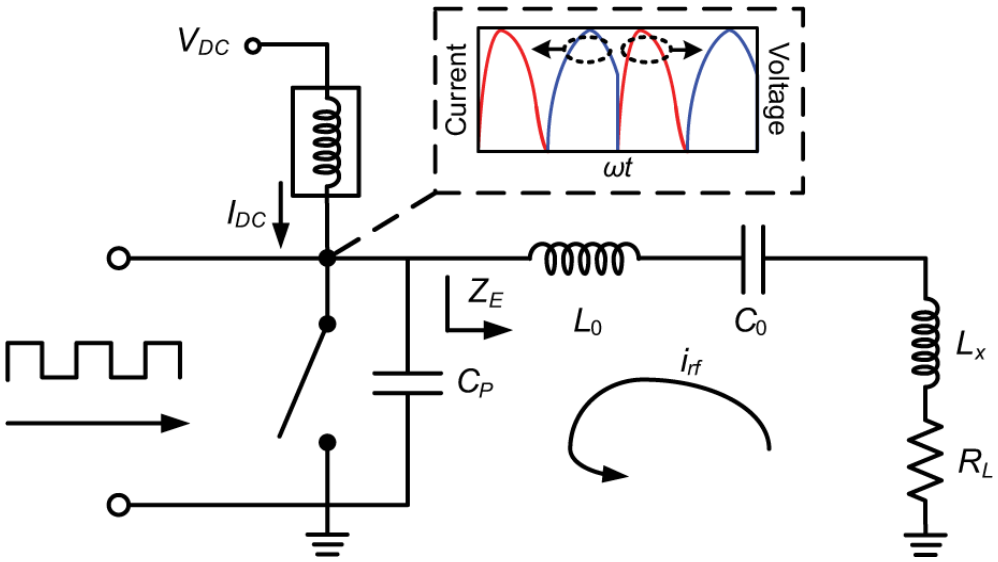


Figure 2.3 Ideal Class E Power Amplifier topology

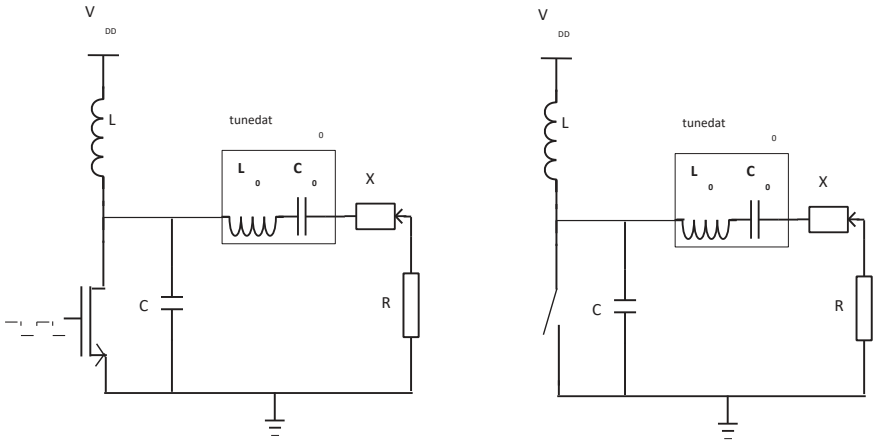
Chun *et al.,* (2012) have illustrated the idea of obtaining high efficiency in power amplifier (PA) with clear analytical equation. They have achieved 2.4GHz PA for

short distance communication by implementing of 0.13μm CMOS technology. Were in the new design methodology class E amplifier is presented witha π- matching output network. The inductance constraint is removed by DC Feed Inductance insteadof RF feed. The measured output power varies from3.2 to 5.7dBm while achieving maximum overall efficiency of about 55% including the auxiliary pre driver stage. The input given to the driver is the CMOS inverter. The circuit is optimized for delivering low output level with high efficiency and allow for fully integrated circuits.

Moreover, Cheng *et al.,* (2013) developed another idea of wafer level bonding of PAaimed at producing a complementary metaloxide semiconductor (CMOS) power amplifier (PA) using a wafer-level bond wire spiral inductor withhigh-quality factor(Q). The inductor with2.75nH inductance achieves a Q of 18, which is three times as much as that of a conventional CMOS standard spiral inductor at 2.4GHz. The Q of the inductor is over 15 from 2 to 14GHz. The output power and power-added efficiency of the PA with the inductor was improved by 1.5dBm and 7% compared to those of the fully integrated CMOSPA.

Acar, (2007) presented the analytical design equations on Class-E power amplifier by taking into account both finite drain inductance and switch on resistance. Based on the analytical solution a coherent non-iterative procedure for choosing the circuit parameters was presented for Class-E PA's with arbitrary duty-cycle and finite dc-feed inductance (e.g. continuously ranging from Class-E with small finite drain inductance to Class-E with RF choke). The obtained analysis results link all known Class-E PA design equations as wellas presenting new design equations. The result of the analysis gives more degrees of freedom to designers in their design and optimization by further expanding the design space of Class-EPA. With used a finite

DC feed inductance instead of RFchoke which can increase η Class E power amplifier by ≈ 30%.



(a) Single-ended Class-E PA (b) Idealized model of single-ended

Figure 2.4 (a) Single-ended Class-E Power Amplifier with Finite DC-Feed Inductance (b) Idealized model of single-ended Class-E Power Amplifier withFinite DC-Feed Inductance

Munir *et al,.* (2008) utilized the ideaof matching network in low power application. They have achieveda fully integrated 2.4GHz class-E power amplifier (PA) with a class-F driver stage. The circuit was fabricated in a standard0.18μm CMOS technology.The results showed a maximum drain efficiency of 38 % and amaximum gain of 17dB,when operating at a 1.2V supply, and the PA delivers anoutput power of 9mW with a power-added efficiency (PAE) of 33%. The supply voltage can go down to 0.6V with an output power of 2 mW and a PAE of 25%. Also the circuit has a second output for testing the effects ofan on-chip filter in the low-power designs. It gives the idea of implementing the power amplifier in biomedical application where a low power consumption is taken into account.

Ray*et al.* (2008) have illustrated the choice of selection of transistor for the broadband design, they utilized the idea of GaNHEMT (Gallium Nitride High Electron Mobility Transistor) characteristics, to compare with other type of transistors. The Analysis of

the transistor such as large signal analysis and small signal analysis were derived and their circuit was simulated using Advanced Design Software (ADS). The transistor modeled was checked using DC Analysis and Load line Analysis.

George *et al.,* (2011) provided technique for the design ofbroadband microwave transistor power amplifiers that utilized the powerful method ofnetwork synthesis to achieve optimum large-signal performance.Only two large-signal transistor measurements per frequency is required to achievea good analytic model of the transistors variation ofadded power with load impedance. Also a mapping function is presented which translates the added-power characteristic into an equivalent linear circuit reflection coefficient characteristic.

Ichiro *et al.,* (2002) have presented Fully Integrated CMOS Power Amplifier Designed Using the Distributed Active-Transformer Architecture. The power amplifier implemented in a low-voltage CMOS process was used to achieves 1.9W output power with 41% efficiency (31% singleended) PAE at 2.4 GHz. It is used as a 450mW 2.4GHz amplifier with27% PAE using a 1V supply. The circuit includes input and output matching to 50Ω, which required no external components. The output matching had been fabricated using 0.35μm CMOS transistors, and it achieved a power added efficiency (PAE) of 41% at this power level.

Babak *et al.,* (2007) achieved a fully integrated 90nm CMOS PA capable of delivering 6.7 dBm of linear power in the 60 GHzband with power amplifier(PA) measured efficiency of 20%, it was appropriate as a pre-driver or for short range mm-wave transmitter applications. This amplifier can be used as a pre-driver or as the main PA for short range wireless communication. The output power had been boosted with on-chip or spatial power combining.

Furthermore, Jee *et al.,* (2010) presented a 2.4 GHz with fully integrated CMOS power amplifier using capacitive cross coupling, fabricated in 0.18 μm CMOS with 3.3V supply voltage. PAE max and PAE at 1dB compression point were 34.3% and 26.8%.

Hajir *et al.,* (2012) have design a fully integrated linearPA using 0.25μm SiGe:C BiCMOS technology at 2 GHz with a supply voltage of 2.5 V. The experimental results show a gain of 13 dB and a maximum output power of 23 dBm with a PAE of 38%.

Namsik *et al.,* (2012) designed an amplifier that operates in saturation mode and regulates its biascurrent. The op-amp has power of 450mW with 1.5Vvoltage, and slew rate of 10volts/us using 0.5 um technology.When the signal is applied the current in the amplifier increases so that these amplifiers generated very high driving current. The op-amp has low power as wellas low voltage.

Shridhar *et al.,* (2013) used 0.13μmbandwidth to achieve output power of 20.028 dBm with highefficiency of 44.669%at 1dB compression pointusing CMOS device for the power amplifier.A cascode topology was used in the driver stage andbasic topology for power stage.

Wei *et al.,* (2004) utalized a 1 W,Class-E power amplifier That implemented on 0.35 μmCMOS technology. 2V at power supply and frequency of 1.98GHz, The poweramplifier was achieved at 48%efficiency.

Maundy *et al.,* (2017) introduced the common-base (or -gate) differential amplifier is revisited and presented. A variant of the same amplifier is also presented and both are analyzed using standard two-port network analysis. Their high frequency behavior, differences in biasing details and noise analysis are also compared and contrasted. New differential input-output filters are derived for the common-base (or -gate)

differential amplifier as well as a new low impedance Norton amplifier. Simulations using Spectre in a 90nm UMC CMOS process of several of the filters aswell as experiments conducted using discrete transistors confirm the theoretical results.

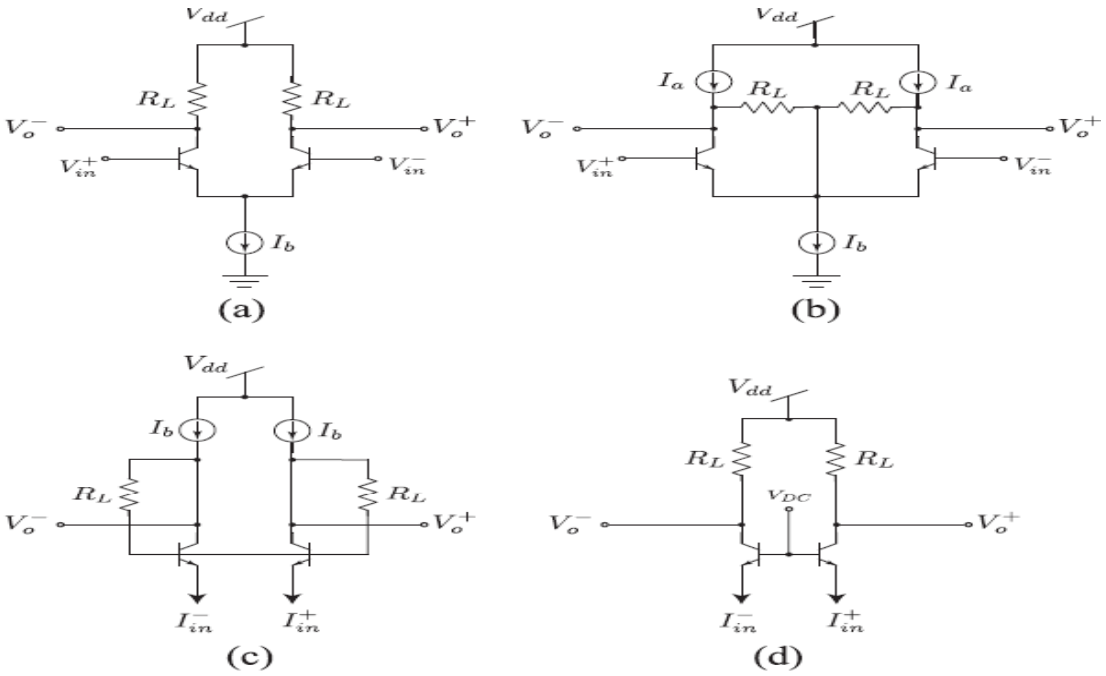


Figure 2.5: (a) The classical differential amplifier (common emitter) using BJTs, (b) an alternative common emitter differential amplifier current biased using BJTs, (c) The proposed commonbase differential amplifier current biased using BJTs and (d) the proposed common-base differential amplifier voltage source biased also using BJTs.

Rahman *et al.,* (2016) presented Class E circuit design for 1MHz application is built by MATLAB Simulink is explained in details and the parameters are determined using related formulas. The circuit is design for 10W application. The efficiency of the simulation for this paper is 81.9%. The user-friendly interface of MATLAB Simulink has advantages in terms of ease of usage and the implementation of the circuit. Which is shown below:

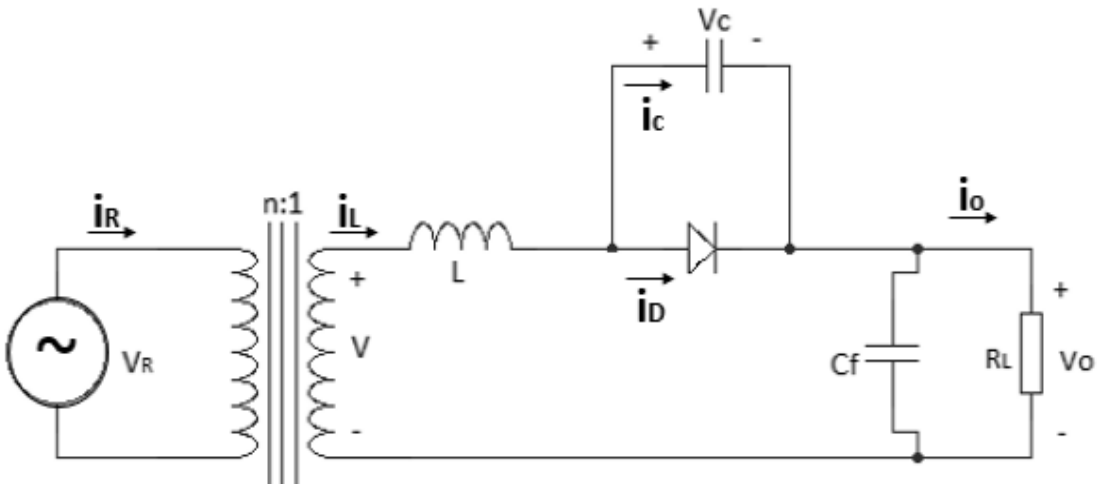


Figure 2.6: Basic circuit of class E power amplifier

Qijin *et al.,* (2016) provided a novel design of high-efficiency broadband power amplifier (BPA) with the low-pass bias networkto enhance theefficiency and output power is presented in this paper. Compared with other bias networks, the proposed low-pass biasnetwork shows a smaller baseband impedance, which can reduce the electrical memory effect. While it provides a largerradio frequency (RF) impedance, which can prevent the leakage of the output power from bias network. A BPA with the proposed bias network is designed using commercial GaN device Cree40025F. The designed BPA shows a fractionalbandwidth of 40%, from 1.8 GHz to 2.7 GHz. The measured results exhibit 73.9 % drain efficiency (DE) value with outputpower of 43.5 dBm at 2.7 GHz, which appears an enhancement of 9.5% and 2.5 dBm comparing with that adopts LC biasnetwork.

David *et al.,* (1995) have achieved a fully integrated Class E power amplifier module operating at 835MHz is designed, fabricated, and tested.The circuit is implemented in a self-aligned-gate, depletion mode0.8-pm GaAs MESFET process. The amplifier delivers 24 dBmof power to the 50-Q load With a power added efficiency greaterthan 50% at a supply voltage of 2.5 V. The power dissipated in the integrated matching networks is 1.5 times the power dissipatedin the transistors.

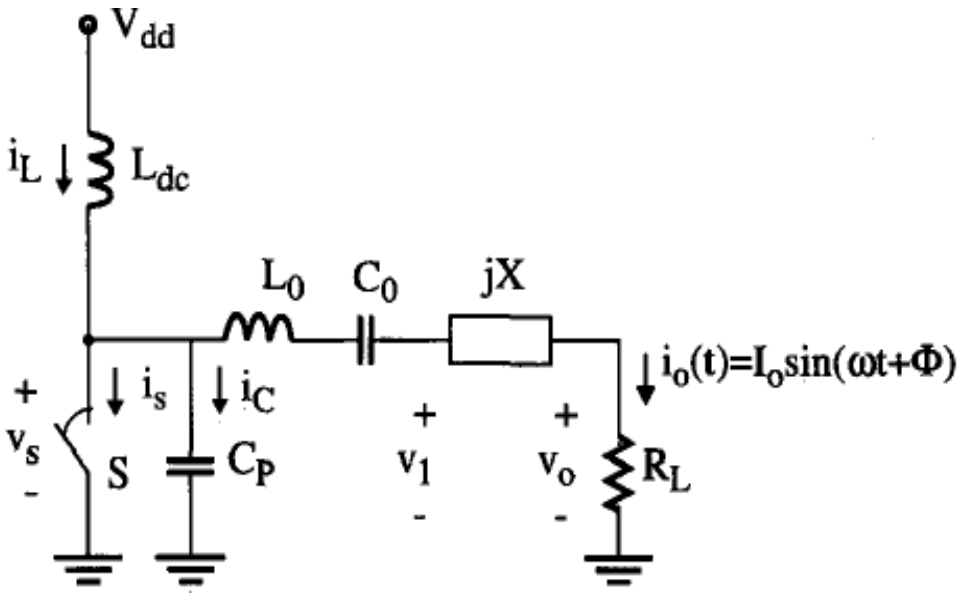


Figure 2.7 Ideal Class E amplifier configuration

Scott *et al.,* (2003). A new family of switching amplifiers, each member having some of the features of both class E and inverse F, is introduced.These class-E/F amplifiers have class-E features such as incorporation of the transistor parasitic capacitance into the circuit,exact truly switching time-domain solutions, and allowancefor zero-voltage-switching operation. Additionally, some numberof harmonics may be tuned in the fashion of inverse class F inorder to achieve more desirable voltage and current waveforms forimproved performance. Operational waveforms for several implementations are presented, and efficiency estimates are compared to class-E.

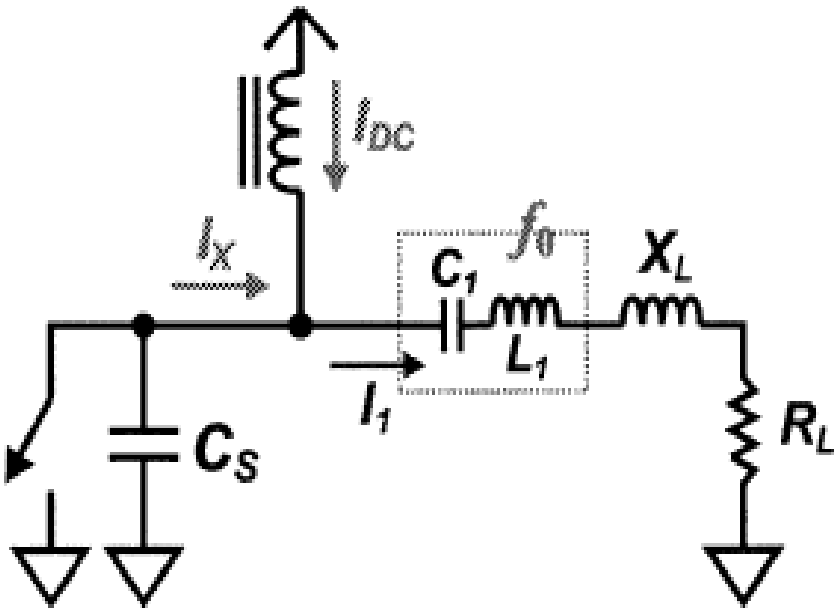


Figure 2.8 Class-E amplifier topology.

Priyanka *et al.,* (2014) utilized VLSI design is one of the paradigms to have low noise, high power and small chip area.The design of CMOS power amplifier is an effort in this domainwhich is applicable for wireless communication system. The proposed design employ switching mode of two stage power amplifier to exploit its soft switching property to achieve high output power and high efficiency.The two stage power amplifier for various communication applications in 65nm CMOS technology is proposed to be designed. The functionality of proposed design oftwo stage power amplifier will be verified for parameters like high output power and high efficiency. The main emphasis is on achieving high gain with low return losses.

Huzaimah *et al.,* (2016) presents the simulation and experimental of Class-E poweramplifier which consists of a load network and a single transistor. Thetransistor is operated as a switch at the carrier frequency of the output signal.In general, Class-E power amplifier is often used in designing a high frequency ac power source because of its ability to satisfy the zero voltage switching (ZVS) conditions efficiently even when working at high frequencies with significant reduction in switching losses. In

this paper, a 10W Class-E power amplifier is designed, constructed, and tested in thelaboratory. SK40C microcontroller board with PIC16F877A is used togenerate a pulse width modulation (PWM) switching signal to drive the IRF510 MOSFET. To be specific, in this paper, the effect on switching and performance at 1MHz frequency are studied in order to understand the Class-E power amplifier behavior. Performance parameters relationships were observed and analysed in respect to the load and duty cycle. The proposedClass-E power amplifier efficiency is 98.44% powered with 12V dc,operated at frequency 1MHz and 50% duty cycle to produce a stablesinusoidal signal. Theoretical calculations, simulation and experimental results for optimum operation using selected component values are then compared and presented. The circuit is shown below:

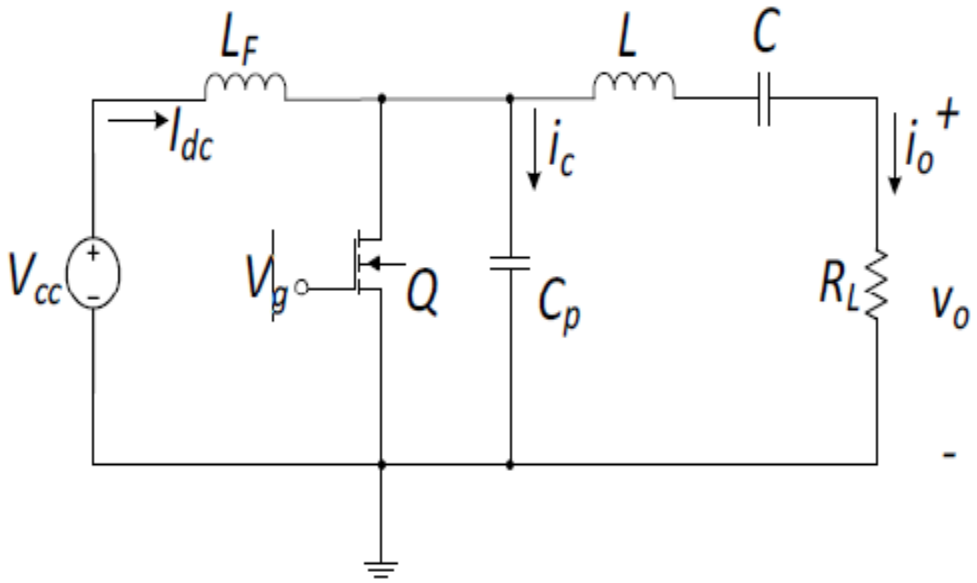


Figure 2.9 Typical Class-E Power Amplifier Circuit

Nadir *et al.,* (2011) they haved investigates how the efficiency of the power amplifier (which is beneficialfor multiple applications in communcation sector) can be improved by increasing the efficiency ofswitching mode class E power amplifiers for frequencies of 900 MHz and 1800 MHz. The paper tacklesmodeling, design improvements and verification through simulation for higher efficiencies. This isthe

continuation of previous work by the authors. These nonlinear power amplifiers can only amplifyconstant-envelope RF signals without introducing significant distortion. Mobile systems such asAdvanced Mobile Phone System (AMPS) and Global System for Mobile communications (GSM) usemodulation schemes which generate constant amplitude RF outputs in order to use efficient but nonlinearpower amplifiers. Improvements in designs are suggested and higher efficiencies are achieved, to thetune of 67.1% (for 900 MHz) and 67.0% (1800 MHz). See the circuit below:

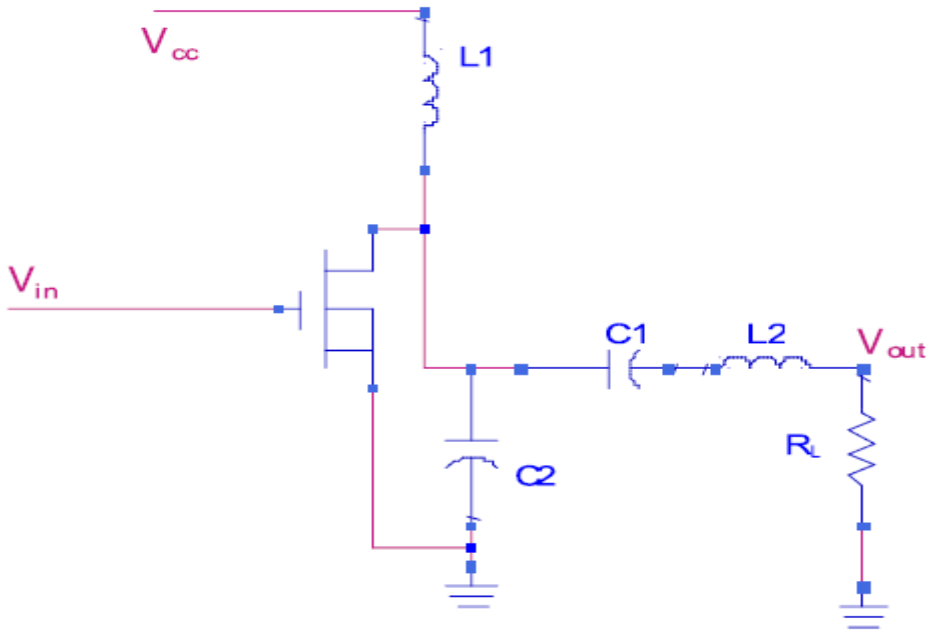


Figure 2.10Basic circuit of class E power amplifier

Reza *et al*., (2010) presents the design of a novel RF poweramplifier (PA) suitable for modern wireless communicationsystems. The PA employs switching mode c1ass-E topology toexploit its soft-switching property to achieve high efficiency. Theuse of another c1ass-E stage as a driver of power stage improvesefficiency and increases the capability of circuit integration. Anew output power control technique is utilized in order to controlthe output power of the proposed P A efficiently by using thearray of switches and capacitors with different sizes. Theproposed PA is simulated by Advanced Design System (ADS) inTSMC 0.18 pm CMOS process and simulation

results show thatthe designed PA can deliver 21.09 dBm output power to 50 0standard load at 2.4 GHz with 57% Power-Added-Efficiency(PAE) from 1.8 V supply voltage and the output power can becontrolled in 1 dBm steps with small drop in efficiency.

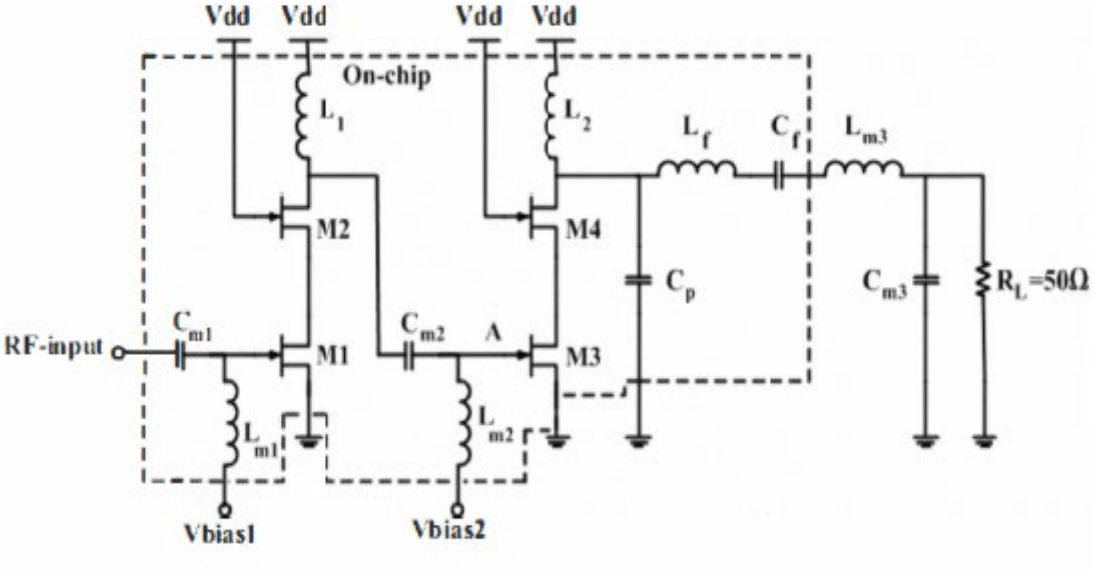


Figure 2.11The proposed c1ass-E power amplifier.

Ping *et al.,* (2007) presented an improved layout and thermal management of eight unit-cells SiGe power HBT with emitter area of 8 _ 0.6 _ 10 lm2were designed for high power density and efficiency performance. The on-wafer power characteristics were measured using an ATN loadpullsystem under class-AB operation at 2.4 GHz. The power HBT achieved a 1-dB compression power (P_1 dB) of 27.3 dBm and a saturationoutput power (Psat) of 30 dBm which was correspond to a power density of 2.6 mW/lm2 for the emitter area. A high peak poweradded efficiency (PAEmax) of up to 75% was obtained, with a power gain of 11.4 dB at a P3-dB of 29.0 dBm. In addition, the real part ofthe source impedance (Rin) was measured to be as high as 28 X. The impedance transfer ratio, Rin/RSystem is only 0.56 which relaxes theneed for a high quality passive component (inductor) for on-chip input matching. This advantage makes it easier for the HBT to be integratedwith other silicon-based transceiver in an RF System-on-Chip (SoC) design.

Ville *et al.,* (2005) provide An integrated two-stage class-E poweramplifier operating at the 2.4 GHz frequency range isdescribed. The implemented power amplifier is capable ofproviding 21.3dBm output power with power addedefficiency of 40 % and gain of 143 d3 at 2.4 GHz. The draineficiency of the class-E power stage is 55 % at 21.3 dBm power, The power amprifier uses 3.3 V supply voltage andwas fabricated with 0.18pm CMOS technology. The linear gain is 23.8dB and the chip area 0.43mm.

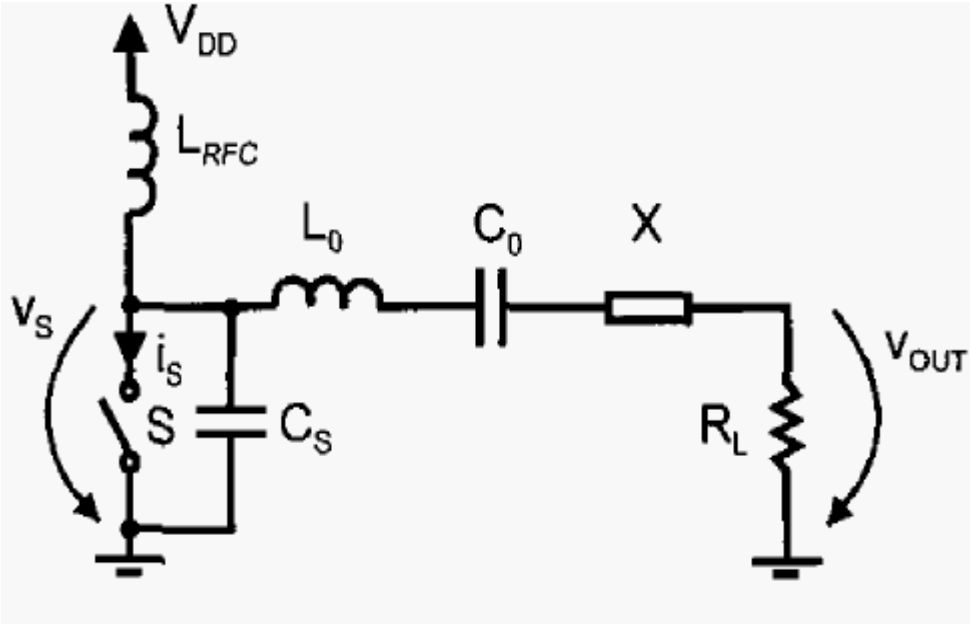


Figure 2.12 Simplified circuit of a class-E power amplifier

Supriya and Ananda (2015) Designed for efficient power amplifier to get output power of 15dbm (32mw) and efficiency of about 70% from input sine wave of amplitude 10mv, at frequency of 2.4 GHz. But obtained result of output power is 14.96dbm(31.39mw) and efficiency is about 66.11% and possible applications of the paper in short distance communication like Wi-Fi, Bluetooth.

Mousa *et al.*, (2013) presented a 1.8 GHz class-E controlled power amplifier (PA). The proposed power amplifier is designed with two-stage architecture. The main advantage of the proposed technique for output control power is a high 37 dB output power dynamic range with good average power adding efficiency. The measurement

results show that the PA achieves a high power gain of 23 dBm and power added efficiency (PAE) by 38%. The circuit was post layout simulated in a standard 0.18µm CMOS technology.

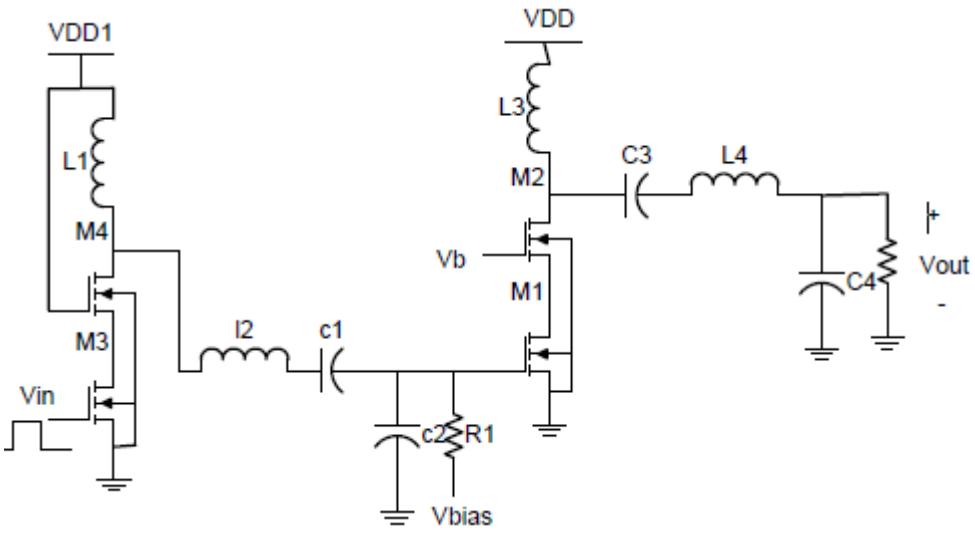


Figure 2.13 Class-E power amplifier schematic.

Lu et al., (2010) presented a new procedure to design of highefficiency class E power amplifiers (*PAs*) using nonlinear transistors. The active device (MESFET-ATF34143) has been investigated and load harmonic networks have also been designed to match the requirement. By using the new procedure, the power added efficiency (*PAE*) of *PA*s could be increased to over 70%. The effect of the stabilized resistors(*Rs*) has also been investigated. Amplifiers in this paper have been designed using PCB FR4 subtract. A good agreement was obtained between the predicted and practical results.

2.3THEORETICAL BACKGROUND

The conventional ideal class EPA topology is depicted in Figure 2.14 showing the basic configuration of Class-E power amplifier (Mader *et al.,* 1998).

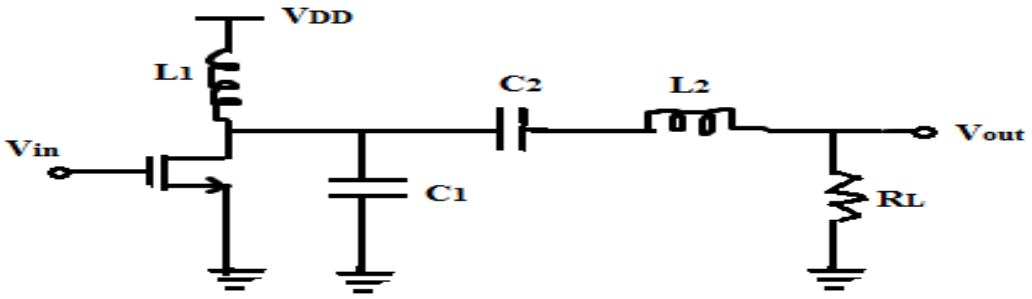


Figure 2.14Basic configuration of class-E PA

The transistor is considered as a switch and capacitor C_I is connected in parallel with it if the transistor switch is turn on, the current flows entirely through the switch drain and source, the voltage is zero. The current can be expressed as

$$I_{sw}(t) = Idc[1 + a\sin(wt + \emptyset)] \qquad 2.1$$

When the switch is turned off, the current flows entirely into the capacitor which is charged simultaneously. During this off state interval, the voltage on this parallel capacitor is given by

$$V_{sw}(t) = \frac{1}{C_I}\int_o^t I_{sw}\,(t^I)\,dt^I$$

$$= \frac{I_{dc}}{WC_I}\,[1 + a(\cos(wt + \emptyset)] \qquad 2.2$$

There are two boundary conditions for the ideal class E operation (Ewing, 1964) referred as zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS) condition.

Assume the switch is turned off at t=0 and turned on at $t = \frac{T}{2}$, those two conditions aregiven by

$$V_{sw}\,(t = 0\,) = 0$$

$$\frac{dV_{sw}}{dt}\,(\,t = \frac{T}{2}\,) = 0 \qquad 2.3$$

Where T denotes the time period of one class E duty cycle. The ZVS condition prevents simultaneous non zero voltage and current across the switch device, the ZVDS enforce the current to start flowing after the voltage has reached zero.

The value of$a$ and $\emptyset$ can be determined uniquely by applying these two constraints leading to

$$a = \frac{\sqrt{1+\pi^2}}{4} 2.4$$

$$\emptyset = \arctan\frac{2}{\pi} \quad 2.5$$

Consequently, there is no overlap between the transient drain current and voltage, which leads to a zero dc power dissipation and 100% drain efficiently. Using Fourier series expansion (Cipriani *et al.* 2008) the optimal fundamental load, yielding perfect class E operation, can be determined by

$$Z_{E,f_o} = \frac{0.28}{Wc_I} e^{49°} \quad 2.6$$

This impedance present inductive, which is illustrated, see figure 1.1. In deal class E mode, the total current through the combined switch capacitor tank is a pure sinusoidal wave, and the harmonics are entirely due to the voltage. The ideal impedances at higher order harmonic frequencies are infinite

$$Z_{E,nf_o} = \infty, \quad n \geq 2 \quad 2.7$$

Sokal *et al,* 1975 performed the original design of the Class-E amplifier assuming idealpassive components and an ideal switching transistor. These approximations lead to thefollowing conditions in the amplifier:

- Choke inductor current i_{LC}will be a DC signal,

- The output current $i_0$will be a perfect sinusoidal waveform, and
- The transistor will turn instantly ON and OFF with zero ON resistance and infinite OFF resistance.

Under these conditions, if the drain voltage and the drain current are never both non-zeroat the same time, then no power will be consumed by the transistor, and with idealpassives, the amplifier will operate at 100% efficiency. In order for this to occur, Sokal *et al,* 1975 stated that the drain voltage and its derivative (the parallel capacitor current i_{CP}times a scalar as shown in equation below) should both be zero at the instant that the transistor turns ON. The voltage must be zero at the time the transistor turns on to prevent power loss, and the derivative should be zero to allow for slight mistuning of the amplifier (sokal *et al.,* 1975). These two conditions have remained as the standard optimal switching conditions for analytical models being developed even today. From the above assumptions, the choke current and the output current can be defined as

$i_{LC} = I_{Dc}$2.8

$$i_0 = \frac{a}{R}\sin(\omega t + \Phi) \qquad 2.9$$

where a is the amplitude of the output voltage, R is the output load resistance and φ is the phase shift between the output voltage and the input signal at the transistor gate. Using KCL at the drain of the transistor yields the equation

$$i_{LC} = i_{CP} + i_D + i_0 \qquad 2.10$$

Since the transistor and the parallel capacitor C_P are in parallel, when the transistor isON, no current flows through C_P. However, when the transistor is OFF, zero can be substituted into eq. 1.10 for i_D with the results of eq. 1.9 yielding

$$i_{CP} = 0 \qquad [ON] \qquad 2.11$$

$$i_{CP} = I_{DC} - \frac{a}{R}\sin(\omega t + \Phi)[\text{OFF}] \quad 2.12$$

Substituting the results of eq. 1.9 into eq. 1.10 along with the result that $i_{CP}=0$ in the ON state yields the drain equations of

$$I_D = I_{DC} - \frac{a}{R}\sin(\omega t + \Phi)\ [\text{ON}] \quad 2.13$$

$$I_{D=0} \qquad [\text{OFF}] \quad 2.14$$

Knowing that a current flowing into a capacitor produces a voltage and knowing that the parallel capacitor voltage is the same as the drain voltage yields the following equationfor the drain voltage v_{DS}

$$V_{Ds} = \frac{1}{C_p}\int_{t=0}^{t} i_{CP}\,dt$$

$$= \frac{1}{C_p}\int_{t=0}^{t}\left(I_{Dc} - \frac{a}{R}\sin(\omega t + \Phi)\right) dt$$

$$= \frac{1}{C_p}\left[I_{Dc}t + \frac{a}{WR}\cos(\omega t + \Phi) - \frac{a}{WR}\cos(\Phi)\right] \quad 2.15$$

The waveforms for these equations can be seen in Figure 1.1. For Figure 1.1, it wasassumed arbitrarily that the transistor is ON for $0 \le \omega t \le \pi$, and OFF for $\pi \le \omega t \le 2\pi$. However, Mustafa *et al.,* (2006) proposed an analytical method tothe design of class-E with finite dc feed inductance. There is a major difference between their analyses and the others. In fact other authors proposed solutions forclass-E with finite dc feed inductance that requires long iterative solution procedure. The great achievement of Mustafa analyze is that it introduce analytical expressionsthat relate the elements and input parameters of this type of class. Based on thatanalytical procedure, relative simple design equations can be found simplifying theclass-E

project.In addition, is known that finite dc feed inductance have significant advantagesif compare with RF choke. As it is explained in (milosevic *et al.,* 2005) and (Grebennikov *et al.,* 2002). The main benefits are:

• Possible to implement on-chip;

• The resistance Ropt has a lower value which implies that output

impedance matching to 50 Ω is easier;

• Supply voltage also can be reduced for the same output power, whichallows the class-E project in low-voltage technologies;

• In the same conditions, it allows larger C shunt value. This condition permits the using of wider transistors with the respectively reducing of it on-resistance, R_{ON}. Naturally Mustafa made some assumptions to start analyze. Some of these are considering the switch ideal and that it has 50 % duty cycle. Therefore when implementing in practice this kind of circuit the designer must have in mind that those design equations are only a first approach to the value of the components. Mustafa presents the following relations between the input parameters (V_{DD}, P_{OUT} and ω) and the circuit components (L_1, C_S, X and R_{OPT}):

$$K_L = \frac{WL_1}{R_{opt}} \qquad 2.16$$

$$K_C = WC_1R_{opt} \qquad 2.17$$

$$K_P = \frac{P_{out}R_{opt}}{VDD^2} \qquad 2.18$$

$$K_L = \frac{X}{R_{opt}} \qquad 2.19$$

The remaining components, L_O and C_O, can be determined from the chosen quality factor:

$$Q_L = \frac{WL_0}{R_{opt}} \quad 2.20$$

Where:

$$W = \frac{1}{\sqrt{L_0 C_0}} \quad 2.21$$

A mathematical analysis similar to (Raab *et al.,* 1977) can be adapted to the case with finite dcfeed inductance. That leads to a relation between K_L, K_C, K_P and K_X with q, where q is:

$$q = \frac{1}{\sqrt{L_1 C_S}} \quad 2.22$$

$$WP_{out} = K_P K_C \frac{Vdd^2}{C_1 {R_{opt}}^2} \quad 2.23$$

The simplest modification to make to the ideal Class-E analysis is to account for thedecay in the transistor at the transition from the ON state to the OFF state. As shown inFigure 1.3, ideally this transition is instantaneous, but in the non-ideal case there is adecay associated with this transition. (Kazimierczuk, 1983) has modeled this as a linearly sloped decreasing line during the OFF state, while (Tu *et al.,* 1999) have more accurately modeled it as an exponential decay in this region which is the approach that will be used in chapter 3. Neither of these papers however completely account for a non-ideal transistor in the fact that they both assume zero ON resistance. The issue of the ON resistance has been addressed by (Choi *et al.,* 1999 Wang *et al.,* 2002, Sekiya *et al.,* 2004,Kessler *et al.,* 2001, Reynaert *et al.* 2003, and Alinikula *et al.,* 2003) although none of theseauthors have accounted for the transistor decay time. (Kessler *et al.,* 2001, Alinikula *et al.,* 2003, and Reynaert *et al.,* 2003) however, have

accounted for the parasitic resistances of thepassive components, while (Reynaert *et al.,* 2003) have also accounted for the finite Q of the output along with (Tu *et al.,* 1999 and Sekiya *et al.,* 2004). With finite output Q, the loadnetwork will not operate as an ideal filter, and additional harmonics besides the fundamental frequency will be present at the output. (Wang *et al.,* 2002, Sekiya *et al.* 2004 and Reynaert *et al.,* 2003) have also accounted for the finite filtering value of the choke inductor L_C. This has the effect of allowing ripple to be introduced onto the i_{LC} waveform as seen in Figure 2.14

2.4 CLASSIFICATION OF POWER AMPLIFIERS:

Power amplifier circuits are classified as A, B, AB, and C,E for switching design.The classification are base on the proportion of each input cycle (conductionangle) during which an amplifying device passes current (Sedra *et al.,* 1998).

2.4.1Class A

Class A power amplifiers show the relatively highest output power, gain andlinearity than any other class mode of operation. On the contrary, its efficiency isthe worst. It is fully conductive as the transistor is never turned off. Thus, it has a 360^0 conduction angle to allow for the always coexistence of drain/collector voltage and current, resulting in huge power dissipation in the transistor(Rabb *et al.,* 2003).

2.4.2 Class B

Class B PAs have less transistor power dissipation than Class A because its gate/base bias is adjusted for drain/collector current cutoff. Therefore, it isconductive a half time in each RF period with 180^0 conduction angle. Power amplifiers in this class suffer from the crossover distortion, which happens when the input signal level is low(Rabb *et al.,* 2003).

2.4.3 Class AB

Class AB PAs have the advantages of both class A and B PAs. It is morelinear than Class B and more efficiency than Class A. In addition, Class AB solves the crossover distortion associated with Class B. Its conduction angle is more than 180^0 (Rabb *et al.,* 2003).

2.4.4 Class C

Class C PAs are less well defined but they are characterized by their conduction angle of less than 180^0. They are still linear, but not as linear as the above three classes. There is usually no bias voltage provided except by the drivesignal, and the highest efficiency Class C PAs can reach is 90%, ideally. They are the most efficient class mode of operation among the transconductance PAs described (Rabb *et al.,* 2003).

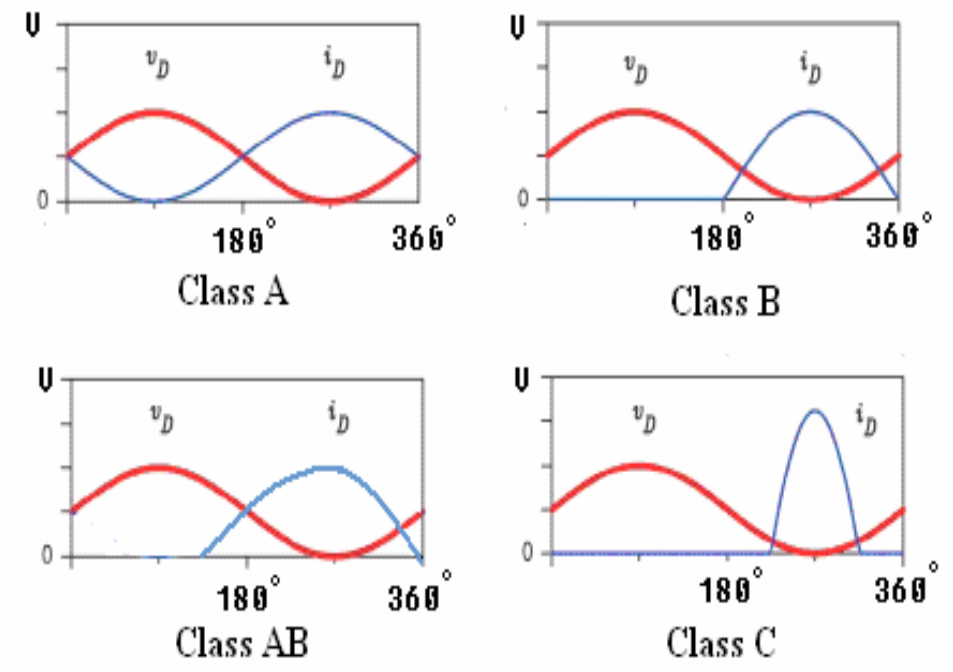


Figure 2.1: Waveforms for Ideal PAs : (a) Class A, (b) Class B, (c) Class AB and(d) Class C (Rabb *et al.,* 2003).

2.5 CLASS-E CIRCUIT COMPOSITION AND FUNCTION

2.5.1 Input Matching

Input matching is required to reduce the reflection due to mismatch betweenthe impedance of the RF input source, the standard 50Ω, and the impedance at the right of 50Ω when looking into the rest of the PA circuit. Let us define the RF power available from the source to be PAV, and the power entering the power amplifier as Pdel. Since the power amplifier is always a part of a complex system, in which it is always preceded and followed by some other devices with specific output power.It is better to have the conjugate match between the RF power available from the generator, or the output power from the device preceding the PA (PAV), and theactual power entering the PA circuit (Pdel), for the purpose of accurately analyzingthe PA and the system's performance, such as efficiency and gain (Tiaotiao, 2007).

2.5.2 Gate Bias

Since the gate voltage variations will drive the switch on and off, the gate biasis important in supplying this swing. For a BJT acting as the switch in class E,the transistor operates incutoff and active region for OFF and ON interval,respectively, each for a half RF switching period. The gate bias should be the DC offset of the voltage waveform, which swings among the values needed for cutoffand active, each for half time. For a FET switch, the transistor operates in cutoffand saturation regions when the switch is in the OFF and ON stage, respectively.Similarly, the gate bias should be the DC level of the swing which makes thetransistor to go cutoff or deep saturation (Tiaotiao, 2007).

2.5.3 Switch

Because the DC gate current is always zero of any MOSFET, the gate biascircuit of a FET is easier to design then that of a BJT. Simply, the gate bias can bea voltage divider composed of the resistors. Thus, FET is used as the switch inthis thesis work .Based on the requirements for frequency and applications, a specific type of FET will be chosen for a specific design. In addition, power output is importantin transistor selection, which is limited by the transistor's drain breakdown voltage and maximum current rating. These two parameters are determined during the manufacturing process and are stated in the datasheet explicitly (Tiaotiao, 2007).

2.5.4 DC Supply

In class E power amplifier operation, the drain voltage will swing up to threetimes of its DC supply voltage, some times even to reach or exceed the breakdown voltage, resulting in the damage to the transistor and the amplifier circuit. Thus,for the safe operation purpose, it is better that drain DC supply is less than a third of the breakdown voltage, and greater than the gate DC bias (Tiaotiao, 2007).

2.5.5 RF Chocks

In class E design, there are two inductors connecting between the DC power supply and the drain, and the bias voltage at the gate and the switch, respectively.They act as short circuits at the DC and open circuits at the operating or the higher frequencies. Thus, they block the RF signals going to the switch; in other words,they only allow a constant D.C current flowing from the DC power to the transistor. Therefore, they are called RF chocks as their function is to "chock" (orblock) RF signals (Tiaotiao, 2007).

2.5.6 Load Network

The load network of Class E prototype proposed by this thesis is composed ofa drain shunt capacitance, a series resonant LC circuit, LC tank circuits for loworder harmonic suppressions, and an output matching network (Tiaotiao, 2007).

2.5.7 Drain Shunt Capacitance

The drain shunt capacitance, C_{shunt}, delays the starting point of the voltage rise section while the current is at the end of its fall section during the ON to OFFtransition. It ensures that at the moment when the switch is turned OFF, the voltage across the switch still remains relatively small as it was still at the end ofthe fall section of the drain voltage, until after the drain current has reached zero.Thus, its purpose is to shape the drain voltage and current waveforms during theON to OFF transition to make certain that there is as little power dissipation by the switch as possible (Tiaotiao, 2007).

2.5.8 Output Matching

Output matching in Class E is usually needed if the required load impedance isother than the standard RF load, 50Ω, associated with small connectors. Because the matching is done between only two real impedances, the simple L-section lumped elements matching circuit can be used.The L-section matching network requires only a capacitor and an inductor.There are two configurations and the applications depend on whether the PA's load resistance is bigger or smaller than 50Ω. But the design equations are thesame (Tiaotiao, 2007).

CHAPTER THREE

MATERIAL ANDMETHOD

3.1 INTRODUCTION

This chapter give a detail of the following materials and method

3.2 MATERIAL

The following materials used for conducting the experiments and simulation are:

IRF540 NMOSFET, 2 Carbon resistor, 2 Electrolytic capacitor, and 2 Inductor, oscilloscope, D.C power supply, Signal generator, Digital Multimeter, 2mm connecting wire, project design board of size 175*67*8mm. A multisim 11.0 electronic simulation software. Some of the above component are already discuss in chapter two.

Oscilloscope, or scope for short, is a device for drawing calibrated graphs of voltagevs time very quickly and conveniently. Such an instrument is obviously useful for the design andrepair of circuits in which voltages and currents are changing with time.

Resistor is an electronic component which resist the flow of current across the resistor.

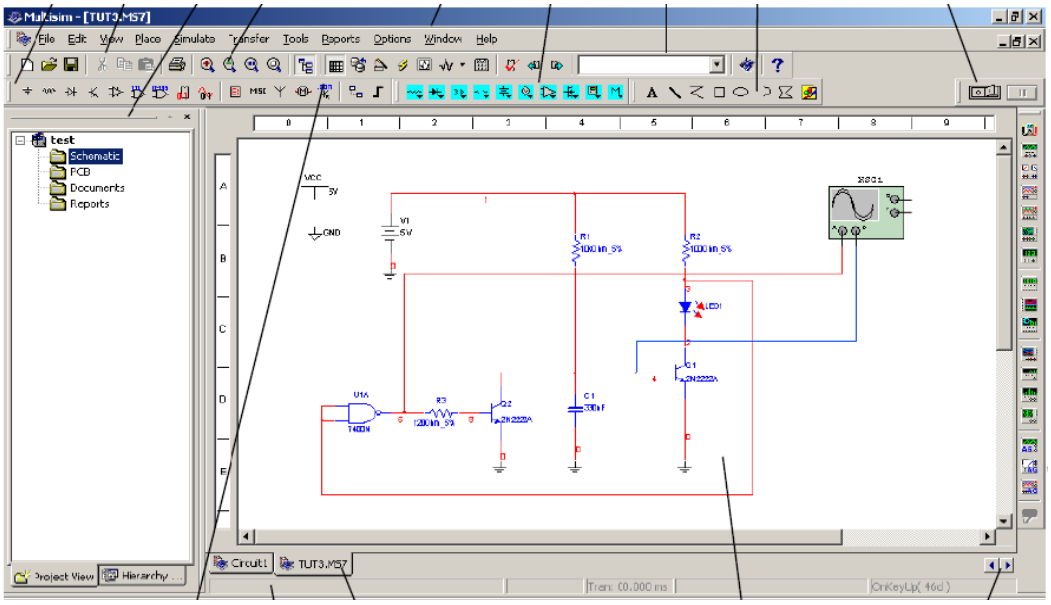


Figure 3.1 Multisim (Maundy *et al.,* 2017)

Menus are where you find commands for all functions.

Standard Toolbar contains buttons for commonly-performed functions.

Instruments Toolbar contains buttons for each instrument.

Component Toolbar contains buttons that let you select components from the Multisimlibraries for placement in your schematic.

Virtual Toolbar contains buttons that let you place virtual components.

Circuit Window (or workspace) is where you build your circuit designs.

Status Bar displays useful information about the current operation and a description of theitem the cursor is currently pointing to.

Project Bar lets you navigate through the different types of files in a project (schematics,PCBs, reports) or to view a schematic hierarchy.

Spreadsheet View allows fast advanced viewing and editing of parameters including component details such as footprints, and design constraints. Users canchange parameters for some or all components in one step and perform a number of other functions.

3.3 DESIGN OF CLASS-E POWER AMPLIFIER

The typical circuit of the Class-E power amplifieris already shown in Figure 2.14 It consists of dc supply voltage source V_{in}, a series-resonant R_L, L_2 and$C_2$and dc choke inductor L_1. They act as short circuits at the DC and open circuits at the higher frequencies. Thus, they only allow a constant DC current flowing from the DC power to the transistor. In the Class-E power amplifier, the switch Q is driven by agate to source voltage Vg. During the switch off interval, the sum of currents through the choke inductance and resonant filter flow through the shunt capacitance. The current through the shunt capacitance produces the switch voltage V_{dd}. The configuration of Class-E power amplifier is illustrated in Figure 3.1.

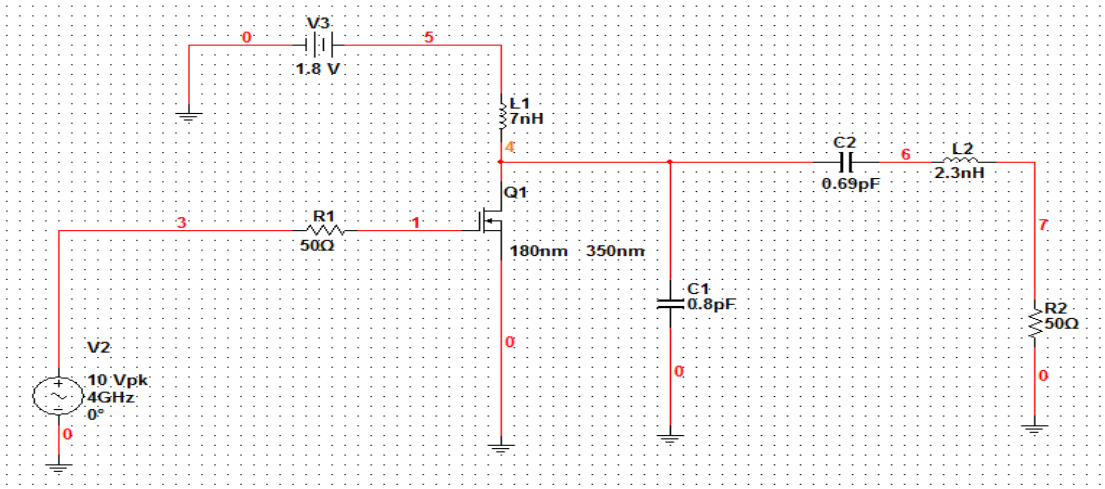


Figure 3.1 schematic diagram of proposed class-E PA

3.4PHYSICAL PRINCIPLES FOR ACHIEVING HIGH EFFICIENCY

Efficiency is achieved at a maximum level by minimizing power dissipation, while providing a desired outputpower (Danaher *et al.,* 2010). Figure 3.2 topology shows conceptual "target" waveforms of transistor voltage and current that meet the high-efficiency requirements. Thetransistor is operated as a switch. The voltage-current product is low throughout the RF period because:

- "On" state: The voltage is nearly zero when high current isflowing, i.e., the transistor acts as a low-resistance "34on"switch during the "on" part of the RF period.
- "Off " state: The current is zero when there is high voltage,i.e., the transistor acts as an"off" switch during the "off"part of the RF period.
- The rise of transistor voltage is delayed until after thecurrent has reduced to zero.
- The transistor voltage returns to zero before the currentbegins to rise. (Kumar *et al*., 2008).

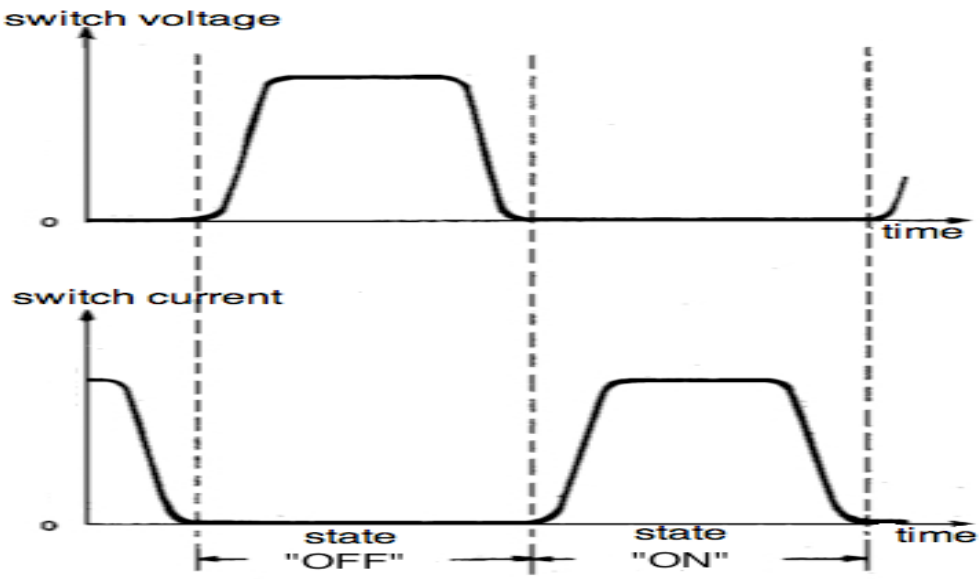


Figure 3.2 Current and voltage waveformfor maximum efficiency (Sokal, 1975)

3.5DESIGN EQUATIONS

For analog design, one need to consider some design constraints. For the design of power amplifier in this work,the output power was 37.4mW, at frequency of 4GHz with 1.8V supply voltage. A non-linear power amplifier was used to achieve high efficiency. Among all classes of non-linear power amplifiers, the class-E power

amplifier demonstrates a unique characteristics which is sophisticated in design with high efficiency performance.

Maximum output power would be calculate as (Supriya and Ananda, 2015).

$$P_{out(\max)} = \frac{0.577Vdd^2}{R_L} = \frac{0.577*(1.8)^2}{50} = 0.0374\text{W} \quad 3.4.1$$

The output matching network is designed to match the output signal of amplifying circuit with antenna.The LC tank circuit is mainly for tuning the output part of the circuit to the operating frequency of 4GHz.The values of tank circuit were calculated with the following relation:

$$\text{f} = \frac{1}{2\pi\sqrt{L_2C_2}} = \frac{1}{2*3.142\sqrt{2.3*10^{-9}}*0.69*10^{-12}} = 3994618972 = 4\text{GHz} \quad 3.4.2$$

$$L_2 = \frac{\pi Vdd^2}{2WP_{out}}\frac{\pi^2-4}{\pi^2+4} = \frac{3.142(1.8)^2}{2*2.5*1010*0.0374}\frac{(3.142)^2-4}{(3.142)^2+4} = 2.3\text{nH} \quad 3.4.3$$

$$\text{W} = \frac{1}{\sqrt{L_2C_2}} = \frac{1}{\sqrt{2.3*10^{-9}}*0.69*10^{-12}} = 2.51*10^{10}\text{rad} \quad 3.4.4$$

$$L_1 = \frac{3.534R_L}{W} = \frac{3.534*50}{2.51*10^{10}} = 7\text{nH} \quad 3.4.5$$

$$C_2 = \frac{1}{L_2W^2} = \frac{1}{2.3*10^{-9}(2.51*10^{10})^2} = 0.69\text{pF} \quad 3.4.6$$

Where F = frequency, W = angular frequency, C_1 and C_2 = Capaitors and L_1 and L_2 = inductors. For the design of perfect input matching, the inductors was connected between the drain and supply. The drain inductance L_1 value was varied accordingly to be tuned at resonance frequency of 4GHz.

$$C_1 = \frac{1}{WR_L} = \frac{1}{2.51*10^{10}*50} = 0.8\text{pF} \quad 3.4.7$$

Input power $P_i = V_i * I_i = 1.8* 0.0208 = 0.0374\text{W}$ 3.4.8

$$Efficiency\ \dot{\eta} = \frac{P_{out}}{P_{in}} * 100\% = \frac{0.0374}{0.0374} * 100\% = 100\% \quad 3.4.9$$

DC Input current $I_i = \frac{8}{\pi^2+4} * [\frac{V_i}{R_i}] = 0.577 * \left[\frac{1.8}{50}\right] = 0.0208A$ 3.4.10

Output current $I_o = \frac{I_i\sqrt{\pi^2+4}}{2} = \frac{0.0208*3.725}{2} = 0.039A$ 3.4.11

Peak voltage across capacitor $VC_2 = \frac{I_0}{WC_2} = \frac{0.039}{2.51*10^{10}*0.69*10^{-12}} = 2.25V$ 3.4.12

Peak voltage across inductor $VL_2 = WL_2I_0 = 2.51 * 10^{10} * 2.3 * 10^{-9} * 0.039$

$= 2.25V$ 3.4.13

Maximum switch current $I_{ms} = [\frac{\sqrt{\pi^2+4}}{2} + 1] * I_i = 2.86*0.0208 = 0.059A$ 3.4.14

Maximum Voltage across switch $V_{ms} = 3.652V_i = 3.652*1.8 = 6.57V$ 3.4.15

The Class-E PAs are classified into different types depending upon the Input and output matching network. Figure 3.3 shows a block diagram of the proposed Class-E power amplifier in this work.

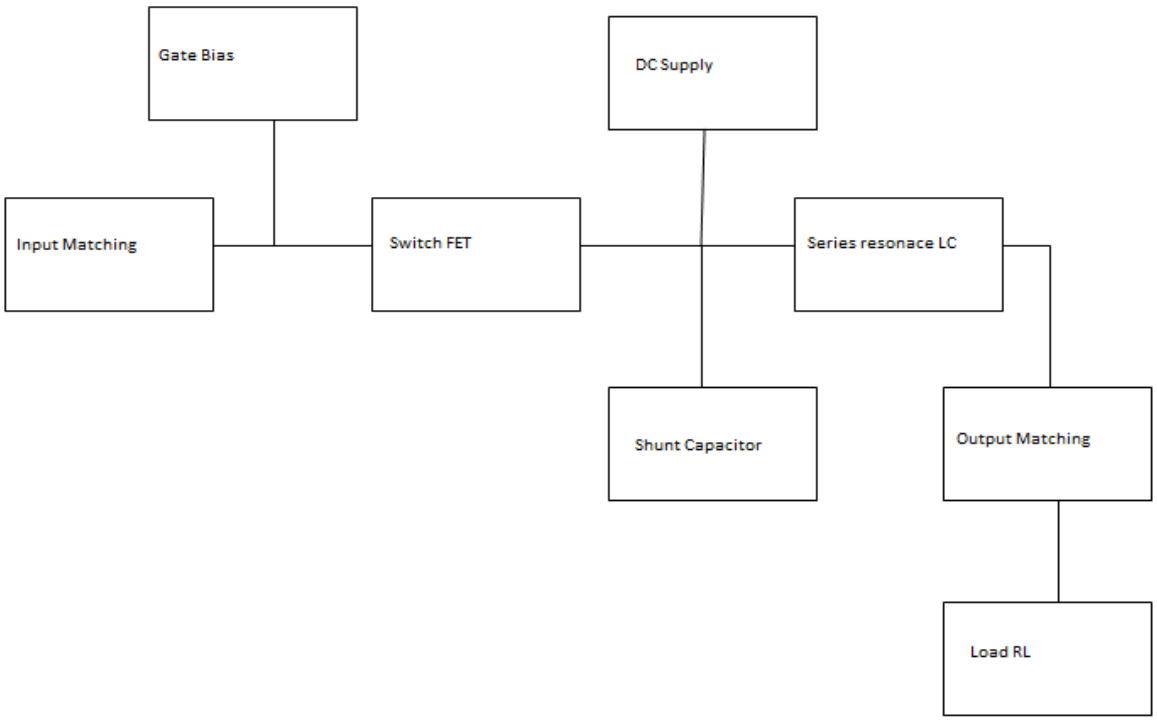


Figure 3.3 Block Diagram of the proposedClass-E Power amplifier

Narrowband amplifier design was choosen in this work for matching network.Narrowbandor bandpass amplifiers are devices whosefrequency responsecharacteristics is determined byresonant LC or RCcircuit. The series LC resonator has a limited frequency response.Resonant LC circuits areplaced in the base and collector circuits of Class-E PA to provide the spectrum-shapingproperties of the amplifier. The resultant bandwidth is dependant on thesharpness of the tuned circuit and the load R_L. The moretuned circuitloaded, the broader its frequency characteristic becomes (Mourlan *et al*., 1965).

CHAPTER FOUR

RESULTS AND DISCUSSION

4.1 INTRODUCTION

This chapter give details of the following results and discussion

4.2RESULTS

The technology used in this calculation, simulation and experiment is 180nm technology. The maximum power added efficiency achieved in this research were: for calculation 100%, experimental 90.34% and simulation 98.42%, the output power was obtained to be 37.4mw with supply voltage of 1.8Vat frequency 4GHz. The comparison is shown in Table 3. The schematic diagram of the designed class-E power amplifier is shown in Fig 3.1.The transient analysis of designed system is shown in Fig 4.2 displaying the input and output voltage.

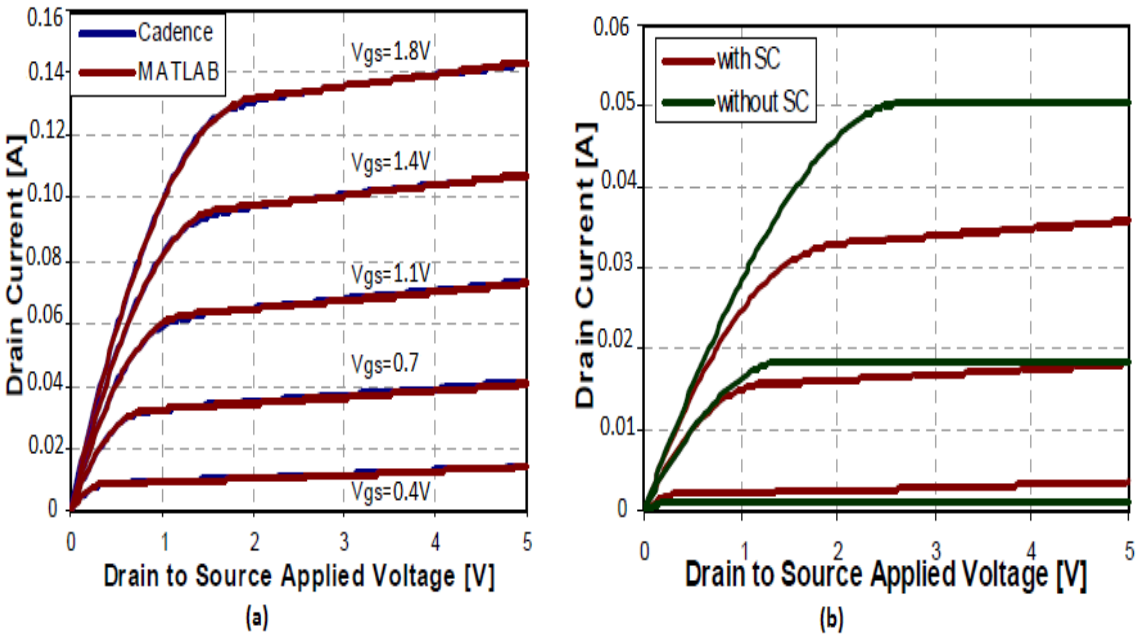


Figure 4.1: IV Characteristic comparison

Table 4.1: Class-E Power Amplifier Comparison

Parameter	Calculated Result	Simulation Result	Experimental Result
R_1 (Ω)	50	50	50
R_2 (Ω)	50	50	50
L_1 (nH)	7	7	7
L_2 (nH)	2.3	2.3	2.3
C1(pF)	0.8	0.8	0.8
C_2 (pF)	0.69	0.69	0.69
$V_{RL\ (peak)}$ (V)	1.933	1.930	1.930
$V_{ds\ (peak)}$ (V)	6.570	6.574	6.574
I_{DC} (A)	0.0208	0.0230	0.0210
$I_{RL\ (peak)}$ (A)	0.039	0.043	0.039
$V_{C\ (peak)}$ (V)	2.25	2.50	2.30
$V_{L\ (peak)}$ (V)	2.25	2.50	2.30
$I_{S\ (peak)}$ (A)	0.059	0.070	0.060
$P_{out\ (a.c)}$ (W)	0.0374	0.0374	0.0374
$P_{i\ (d.c)}$ (W)	0.0374	0.0380	0.0414
η (%)	100	98.42	90.34

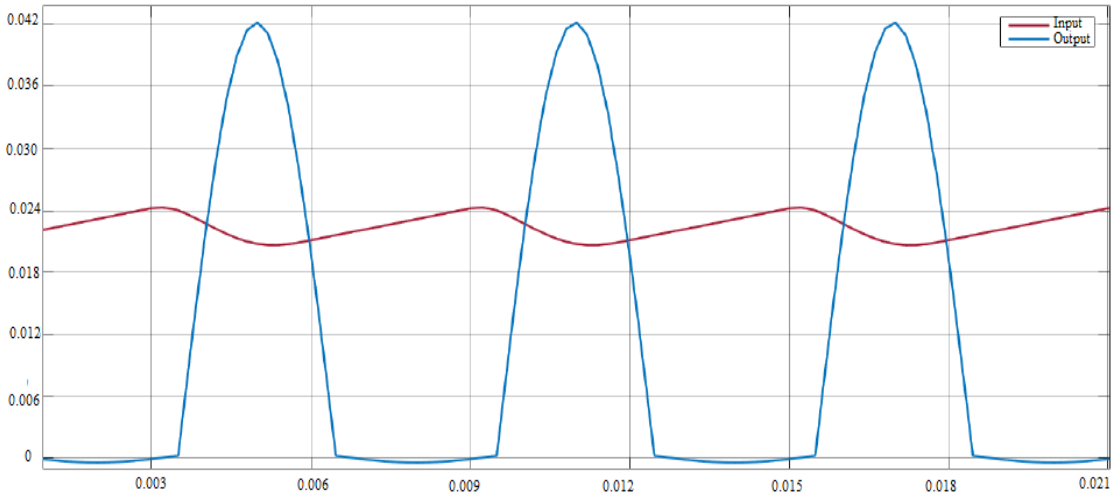


Figure: 4.2Input and Output currents of the circuit.

Table 4.2: Class-E Power Amplifier with variation of R_1, R_2, L_1, L_2, and C_1, C_2.

Parameter	Experiment (1)	Experiment (2)	Experiment (3)
R_1 (Ω)	70	70	8.31
R_2 (Ω)	50	60	8.31
L_1 (nH)	7	10	57.60
L_2 (nH)	2.3	4	13.22
C_1 (pF)	1	3	3.52
C_2 (pF)	1	2	2.17
$V_{RL\ (peak)}$ (V)	1.93	1.93	1.93
$V_{ds\ (peak)}$ (V)	6.574	6.574	6.574
I_{DC} (A)	0.031	0.02	0.13
$I_{RL\ (peak)}$ (A)	0.058	0.032	0.023
$V_{C\ (peak)}$ (V)	2.31	0.62	4.3
$V_{L\ (peak)}$ (V)	2.35	3.2	77.3
$I_{S\ (peak)}$ (A)	0.09	0.06	0.04
$P_{out\ (a.c)}$ (W)	0.0374	0.0312	0.225
$P_{i\ (d.c)}$ (W)	0.056	0.036	0.234
η (%)	67	87	96

Table 4.3: Comparison of designed system with referred papers

Reference	This work	Ding,Y. 2005	Park et al. 2007	Donald et al. 2009	Lee et al. 2010	Supriya, M. 2015
Technology	180nm	180nm	180nm	180nm	180nm	180nm
Supply Voltage	1.8V	1.8V	1.8V	1.8V	3.3V	1.8V
Frequency	4GHz	2.4GHz	1.9GHz	2.4GHz	1.8GHz	2.4GHz
Output Power	37.4mW	22dBm	1.6W	20dBm	2W	32Mw
Efficiency	98.42%	44%	40%	62%	31%	66.11%

4.3 DISCUSSION

Based on the design equations and assumptions provided in Section 3, all the circuit parameters were calculated and tabulated in Table 4.1.Then simulations were carried out using Multisim 11.0 before the implementation of the real circuit. In order to validate the simulation results,the experimental work was carried out. IRF540 MOSFET (nchannel,enhancement mode) was used as a switching device in the design.Based on Table 4.1 and Table 4.2, the peak switch voltage and current were 6.57V and 0.059A respectively. According to IRF 540 MOSFET datasheets,the breakdown switch voltage and current were 100V and 28A respectively. This confirms that the IRF540 MOSFET is suitable to be used for Class-E power amplifier circuit. All the voltage and current of the designed amplifier were measured by Digital Multimeter and oscilloscope was used to obtain the waveforms data of the output

voltage.By analyzing and comparing both results from the calculation and simulation. The efficiency of the overall system of power input $P_i$to power output, P_o based on the particular values was determined. It can be shown that the efficiency of Class E simulation circuit and experiment in Table 4.1differs by1.58% and 9.66% from the efficiency calculated theoretical values. This situation happened because the value of components used for the simulation is selected as the best values to suit for the zero-voltage switching (ZVS) condition. Beside, Multisim is very sensitive towards decimal points of the values. Therefore, some values are rounded to acceptable ones to make the simulation results firmly presented.

CHAPTER FIVE

SUMMARY, CONCLUSION AND RECOMMENDATION

5.1 SUMMARY

Design and analysis of class-E power amplifier a 4GHz band for mobile application is introduced. This work designed Class-E power amplifier with load network and a single transistor without excessive reactance at higher frequency to solve the problems such as: Power dissipation in the active device, Variation in supply voltage and Inductance constraint using Narrow band amplifier design.

5.2 CONCLUSION

The model of Class-E Power amplifier is designed and presented in this research work. It is proved successful through verification in the multisim circuit simulator. Deriving an expression to obtain thecorrect optimal switching condition was carried out in order to prove this theory correct. The calculation 100%, simulation 98.42% and experimental 90.34% design of Class-E poweramplifier with load network and a single transistor was carried out, the overall efficiency were achieved, powered with 1.8V dc. The amplifier was operated at band frequency of 4GHz and 50% duty cycle for a stablesinusoidal signal.Therefore, it can be concluded that the optimum operation can be achieved only at an optimumload resistance,$R_2 = R_1$. at $R_2 = R_1$the sinusoidal output voltage will reach nearly to maximum forthe tested operating frequency.

5.3 RECOMMENDATION

Future work associated with this research could be done in the area of the optimalswitching conditions. Sokal *et al.,* (1975) assumed that the drain voltage should return all the way to zero volts at the switching points since that was the

assumed ON state drain voltage of the transistor. Another Derivingan expression to obtain the correct optimal switching condition would require significant calculation in order toprove this theory correct, and will be left for future work.

5.4 CONTRIBUTION TO KNOWLEDGE

Class-E power amplifier without excessive reactance at higher frequency was design, it was found that the efficiency of design Class-E PA is differ by 32.31% of which the total efficiency obtained is 98.42% compared to the previous work done using the same 180nm technology.

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